Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please amend claims 34 and 42, and add new claims 50-52 as follows:

Listing of Claims:

1-33. (Canceled)

34. (Currently Amended) A board-on-chip (BOC) and lead-on-chip (LOC) semiconductor device package assembly, comprising:

a semiconductor die;

a substrate to which the semiconductor die is attached;

a tri-layer die attach tape comprising adhesive die attach material disposed between the semiconductor die and the substrate, the adhesive die attach material directly abutting the substrate and the semiconductor die, a die attach bondline at the interface between the adhesive die attach material and the semiconductor die being substantially void free and outgassed under isostatic pressure effective to substantially raise a boiling point of a solvent of the adhesive die attach material.

35. (Canceled)

36. (Original) The semiconductor device package assembly of claim 34, further comprising a lead frame disposed between the semiconductor die and the substrate.

37. (Original) The semiconductor device package assembly of claim 34 wherein the semiconductor die is electrically coupled to conductive traces formed on the surface of the substrate through conductive bond wires.

38-41. (Canceled)

42. (Currently Amended) A board-on-chip (BOC) and lead-on-chip (LOC) semiconductor device package assembly, comprising:

a semiconductor die;

a substrate having a first surface and a second surface, and an aperture disposed therethrough;

a pressure and heat cured tri-layer die attach tape cured at an elevated temperature under isostatic pressure effective to substantially raise a boiling point of a solvent of the tri-layer die attach tape, the tri-layer attach tape comprising adhesive die attach material disposed between the semiconductor die and the first surface of the substrate to adhere the die to the first surface of the substrate, a die attach bondline at the interface between the semiconductor die and the first surface of the substrate being substantially void free, and

a plurality of bond pads disposed on the semiconductor die and aligned with the aperture, the bond pads being electrically coupled to a corresponding plurality of conductive leads formed on the second surface of the substrate by bond wires passing through the aperture.

43. (Canceled)

44. (Previously Presented) The semiconductor device package assembly of claim 42, further comprising a lead frame disposed between the semiconductor die and the substrate.

45. (Previously Presented) The semiconductor device package assembly of claim 42 wherein the semiconductor die is electrically coupled to conductive traces formed on the surface of the substrate through conductive bond wires.

46-49. (Canceled)

50. (New) The semiconductor device package assembly of claim 42, wherein the pressure and heat cured tri-layer die attach tape comprises tri-layer die attach tape cured at a temperature between 100 and 200 degrees Celsius under isostatic pressure of between 30 and 250 p.s.i..

51. (New) The semiconductor device package assembly of claim 50, wherein the pressure and heat cured tri-layer die attach tape comprises tri-layer die attach tape cured at a temperature between 140 and 175 degrees Celsius under isostatic pressure of between 125 and 165 p.s.i..

52. (New) The semiconductor device package assembly of claim 51, wherein the pressure and heat cured tri-layer die attach tape comprises tri-layer die attach tape cured at a temperature of about 165 degrees Celsius and an isostatic pressure of 125 p.s.i..